Experiment 5



American International University- Bangladesh

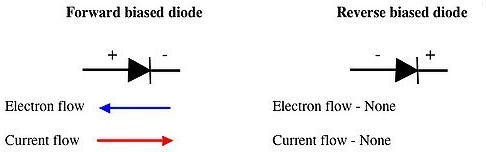
Department of Faculty of Engineering

EEE 3102: Digital Logic & Circuits Laboratory

# Title: Construction of Diode and Transistor Logic Gates

**Part I: Construction of Diode Logic Gates Introduction:**

A diode is a two-terminal electrical device that allows current to flow in one direction but not the other. It is like a pipe with an internal valve that allows water to flow freely in one direction but shuts down if the water tries to flow backward. The diode's two terminals are called the anode and cathode. In the diode symbol, the arrow points from the anode (flat part of triangle) toward the cathode (point of the triangle).



The device operates by allowing current to flow from anode to cathode, basically in the direction of the triangle. Recall that current is defined to flow from the more positive voltage toward the more negative voltage (electrons flow in the opposite direction). If the diode's anode is at a higher voltage than the cathode, the diode is said to be forward biased, its resistance is very low, and current flows. If the anode is at a lower voltage than the cathode, the diode is reverse-biased, its resistance is very high, and no current flows. The diode is not a perfect conductor, so there is a small voltage drop, approximately 0.7 V, across it.

In this group of experiments we will implement some logic functions using the DL circuits and discover the potential benefits and problems of using the DL logic.

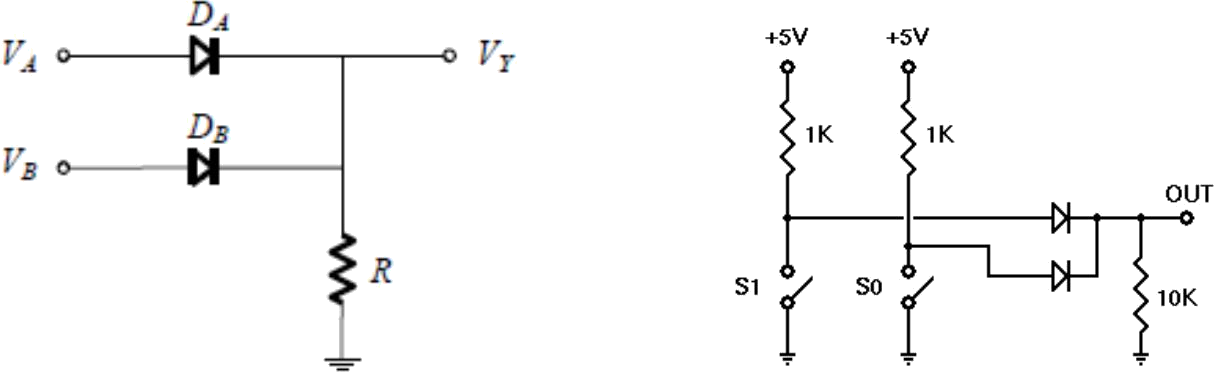
# Theory and Methodology:

## Diode Logic OR Gate:

A Diode Logic OR gate consists of nothing more than diodes (one for each input signal) and a resistor. Here, the 10KΩ resistor (R) is added to provide a ground reference for the output signal. If there are no input signals connected to the diodes, the output will be ground, or logic 0. Thus, an open input is equivalent to a logic 0 input, and will have no effect on the operation of the rest of the circuit.

It is possible to add any number of input diodes to this circuit, each with its separate input signal. However, two inputs are quite sufficient to demonstrate the operation of the circuit.

|  |  |
| --- | --- |
| (a) | (b) |
| Fig.1 DL-OR Gate | |

Assuming the diodes are ideal, the voltage truth table as given in Table 1(a) is obtained. The corresponding logic truth table is given in Table 1(b):

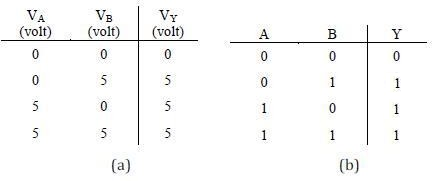


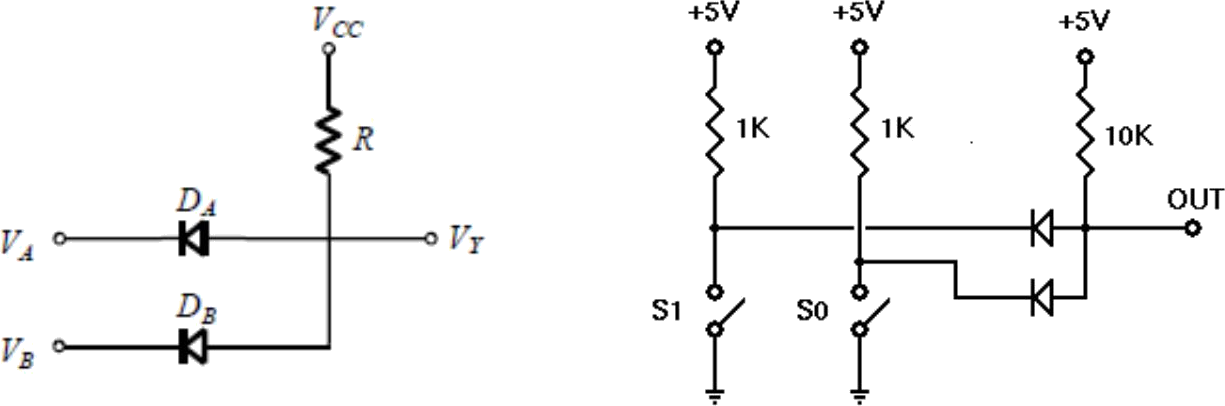
Table 1

## Diode Logic AND Gate:

A Diode Logic AND gate consists of diodes (one for each input signal) and a resistor. As with the DL OR gate, the 10KΩ resistor (R) provides a reference connection. Unlike the OR gate, however, this is a reference to +5 volts, rather than to ground. If there are no input signals connected to the diodes, the output will be +5 volts, or logic 1. Thus, an open input will not affect the rest of the circuit, which will continue to operate normally.

As with DL-OR gates, it is possible to add any number of input diodes to this circuit, each with its separate input signal. However, two inputs are quite sufficient to demonstrate the operation of the circuit.

(a)



(b)

Fig.2 DL-AND Gate

Assuming the diodes are ideal, the voltage truth table of the above AND gate is as given in Table 2(a). The corresponding logic truth table is in Table 2(b).

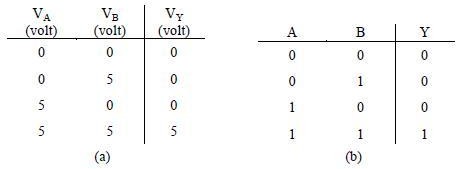


Table 2

## Two-Input DL AND –OR Gate:

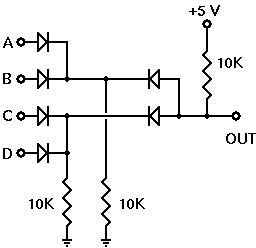
After looking at both the Diode Logic (DL) OR gate and AND gate and evaluating whether their operations were within acceptable parameters, the AND and OR gates will be cascaded. The OR gate will be used to combine the outputs of two AND gates and how well this combination works will be observed.

Fig.3 DL-AND-OR Gate

**Diode polarity:**

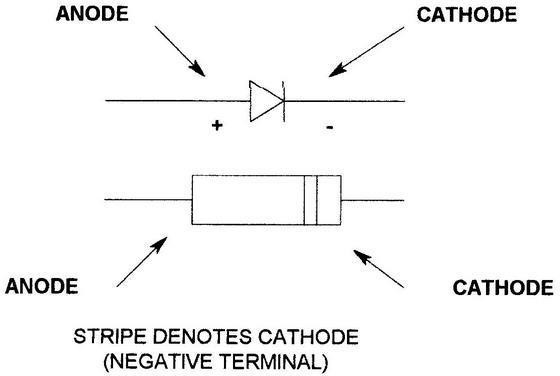


Fig.4 Diode polarity

# Pre-Lab Homework:

1. Explain how a p-n junction or diode works? When does it conduct?

Ans:

* In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero. See figure 4.1.

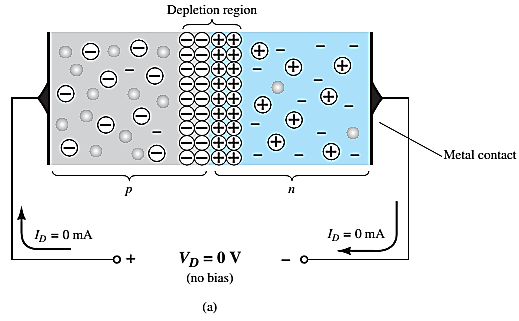


Figure 4.1: p-n junction with NO external bias

* The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by Is .

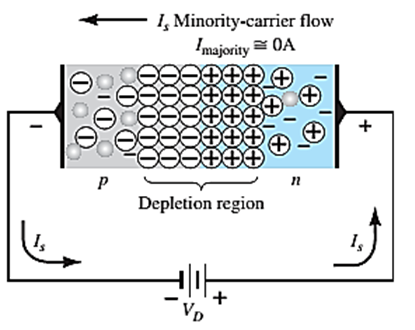


Figure 4.2: Reverse Biased p-n junction

* It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be referred to as Shockley’s equation.

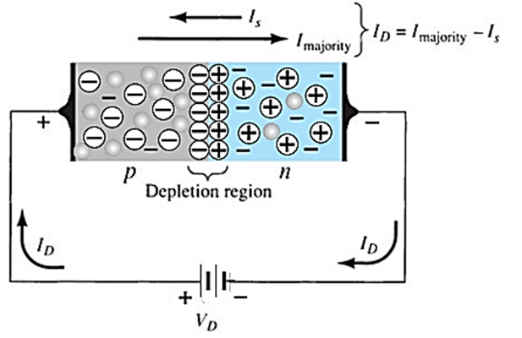


Figure 4.3: Forward biased p-n junction

1. What is a wired logic?

Answer: A wired logic connection implements logic (boolean algebra) using only passive components like resistors and diodes. This logic connection can create an OR , an AND gate but it cannot create NOT gate.

1. Explain the operation of depletion region for different biasing conditions.

Answer: In p-type semiconductors, holes are the majority charge carriers while free electrons are the minority charge carriers. On the other hand, in n-type semiconductors free electrons are the majority charge carriers while holes are the minority charge carriers. See figure 4.1. If p-type semiconductor is joined with n-type semiconductor, a p-n junction is formed. The region in which the p-type and n-type semiconductors are joined is called p-n junction. This p-n junction separates n-type semiconductor from p-type semiconductor. In n-type semiconductors, large number of free electrons is present due to this they get repelled from each other and try to move from a high concentration region (n-side) to a low concentration region (p-side). Moreover, near the junction free electrons and holes are close to each other. According to coulombs law there exist a force of attraction between opposite charges. Hence, the free electrons from n-side attracted towards the holes at p-side. Thus, the free electrons move from n-side to p-side. Similarly, holes move from p-side to n-side. The free electrons that are crossing the junction from n-side provide extra electrons to the atoms on the p-side by filling holes in the p-side atoms. The atom that gains extra electron at p-side has more number of electrons than protons. We know that, when the atom gains an extra electron from the outside atom it will become a negative ion. Thus, each free electron that is crossing the junction from n-side to fill the hole in p-side atom creates a negative ion at p-side. Similarly, each free electron that left the parent atom at n-side to fill the hole in p-side atom creates a positive ion at n-side.

Negative ion has more number of electrons than protons. Hence, it is negatively charged. Thus, a net negative charge is build at the p-side of p-n junction. Similarly, positive ion has more number of protons than electrons. Hence, it is positively charged. Thus, a net positive charge is build at n-side of the p-n junction.

The net negative charge at p-side of the p-n junction prevents further flow of free electrons crossing from n-side to p-side because the negative charge present at the p-side of the p-n junction repels the free electrons. Similarly, the net positive charge at n-side of the p-n junction prevents further flow of holes from p-side to n-side. Thus, immobile positive charge at n-side and immobile negative charge at p-side near the junction acts like a barrier or wall and prevent the further flow of free electrons and holes. The region near the junction where flow of charges carriers are decreased over a given time and finally results in empty charge carriers or full of immobile charge carriers is called depletion region. The depletion region is also called as depletion zone, depletion layer, space charge region, or space charge layer. The depletion region acts like a wall between p-type and n-type semiconductor and prevents further flow of free electrons and holes.

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

# Apparatus:

1. 10K ohm resistor (brown-black-orange).
2. 1N914/1N4002 diodes or equivalent.
3. Connecting wires.
4. Trainer Board

# Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within VDD) to turn on the transistors and/or chip, otherwise it may get damaged.

# Experimental Procedure:

* 1. Construct the DL-OR gate on your breadboard as shown in Fig. 1. Then draw a Truth Table similar to the one provided and fill in your experimental results.
  2. Construct the DL-AND gate on your breadboard as shown in Fig. 2. Then draw a Truth Table similar to the one provided and fill in your experimental results.
  3. Construct the DL-AND-OR gate on your breadboard as shown in Fig. 3. Before beginning the experiment, calculate your expected results for all the different input combinations and put them

in a Truth Table similar to the one provided. Then draw a second Truth Table and fill it with your experimental output values.

# Results and Discussion:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

**Report:**

1. For, each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?

Answer:

For Diode Logic OR gate:

If one or both inputs are at logic “1” (5 volts), the current will flow through one or both diodes. This current passes through the resistor and causes the appearance of a voltage across its terminals, thereby obtaining logic “1” on the output. See figure 1. We only get logic “0” (0 volts) on the output when both inputs are in logic “0”. In this case, the diodes do not conduct, there is no current through the resistor R and there is no voltage across its terminals. As a result, the voltage at Vout is the same as ground (0 volts)

For Diode Logic AND gate:

When both inputs are at logic “1″, the two diodes are reverse biased and there is no current flowing to ground. Therefore, the output is logic “1” because there is no voltage drop across the resistor R. If one of the inputs is logic “0”, the current will flow through the corresponding diode and through the resistor. Thus, the diode anode (the output) will be logic “0”. This method works fine when the circuits are simple, but there are problems when you have to make interconnections with such gates. See Figure 2.

For Diode Logic OR and AND gate:

We made a connection of 2 AND gates and 1 OR , as shown on the picture. If we analyze carefully the picture, we notice that one of the two AND gates outputs will be in logical “1” (high level), when the A and B inputs or the C and D inputs are in logical “1” (high level). These outputs serve as inputs for the OR gate.

Analyzing the output of the OR gate and assuming that the values of the resistors are the same throughout the circuit, a voltage division has been created, then the output voltage will be approximately: Vout = (+V -Vd)/2.

Vd= Diode voltage drop

By replacing V and Vd with real values on the last formula we get: Vout = (5-0.7)/2 = 2.15 Volts. (We divide it by 2 because there are two resistors of equal value on the electric current flow).

In the case in which all inputs (A, B, C, D) are on logical “1”, the two resistors of the AND gates would be in parallel, and they would be in series with the OR gate resistor. This would provide an output voltage of 2.85 Volts. This level is in the not allowed (prohibited) area for a logical “1”.

If we put more gates in cascade the problem will be more serious, so this method is only used for simple gates. See figure 3.

1. Why are diode logic gates not suitable for cascading operation?

Answer: One of the reasons is the forward voltages of the diodes (usually about 0.7V) will add up if we put them in series. If we are using AND gates, where we have a diode on every input which pulls down the output when the input voltage goes low, with a single gate, minimum output voltage will be 0.7V, which is within the range of a TTL logic 0 state (0 - 0.8V). we can use 2 gates in series and the minimum voltage will be 1.4V, which is an indeterminate logic state. The other reason is that the pull-up or pull-down resistor in the diode logic gate makes it a high output resistance device. If we try to drive another diode logic gate with it, the output voltage of the first gate will be affected by the resistor in the second gate. A diode logic gate should always drive a high input resistance input.

# Part 2: Construction of Bipolar Transistor Logic Gate Introduction:

A bipolar transistor is a three-terminal semiconductor device. Under the control of one of the terminals, called the base, current can flow selectively from the collector terminal to the emitter terminal.

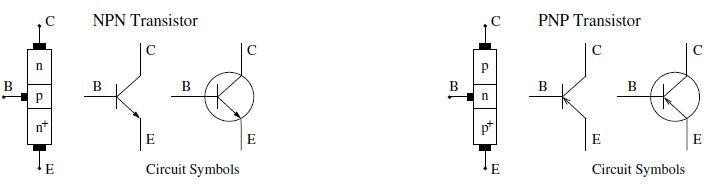


Fig 5: Bipolar junction transistor circuit symbols

In this experiment we examine how to build logic gates from bipolar transistors using the RTL, DTL and TTL design.

**Theory and Methodology:**

## Resistor-Transistor Logic (RTL):

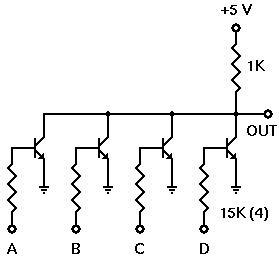
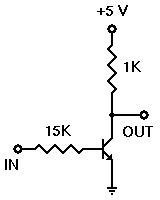
Resistor-Transistor Logic (RTL) is a large step beyond Diode Logic (DL). Basically, RTL replaces the diode switch with a transistor switch. If a +5v signal (logic 1) is applied to the base of the transistor (through an appropriate resistor to limit base-emitter forward voltage and current), the transistor turns fully on and grounds the output signal. If the input is grounded (logic 0), the transistor is off and the output signal is allowed to rise to +5 volts. In this way, the transistor not only inverts the logic sense of the signal, but it also ensures that the output voltage will always be a valid logic level under all circumstances. Because of this, RTL circuits can be cascaded indefinitely, where DL circuits cannot be cascaded reliably at all.

Fig.6: RTL Inverter Fig .7: 4-input RTL Inverter

## Diode-Transistor Logic:

Diode–Transistor Logic (DTL) is a class of digital circuits built from bipolar junction transistors (BJT), diodes and resistors; it is the direct ancestor of transistor–transistor logic (TTL).

DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed (especially in comparison to TTL).

RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

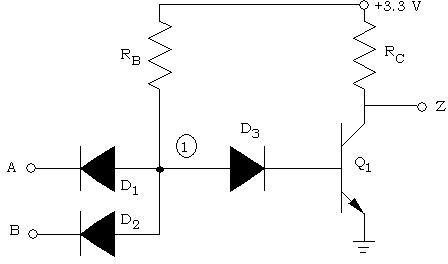


Fig 8: 2-input DTL NAND Gate

## Transistor-Transistor Logic:

We can think of a bipolar transistor as two diodes placed very close together, with the point between the diodes being the transistor base. Thus, we can use transistors in place of diodes to obtain logic gates that can be implemented with transistors and resistors only; this is called transistor-transistor logic (TTL).

One problem that DTL doesn't solve is its low speed, especially when the transistor is being turned off. Turning off a saturated transistor in a DTL gate requires it to first pass through the active region before going into cut-off. Cut-off, however, will not be reached until the stored charge in its base has been removed. The dissipation of the base charge takes time if there is no available path from the base to ground. This is why some DTL circuits have a base resistor that's tied to ground, but even this requires some trade-offs. Another problem with turning off the DTL output transistor is the fact that the effective capacitance of the output needs to charge up through Rc before the output voltage rises to the final logic '1' level, which also consumes a relatively large amount of time. TTL, however, solves the speed problem of DTL elegantly.

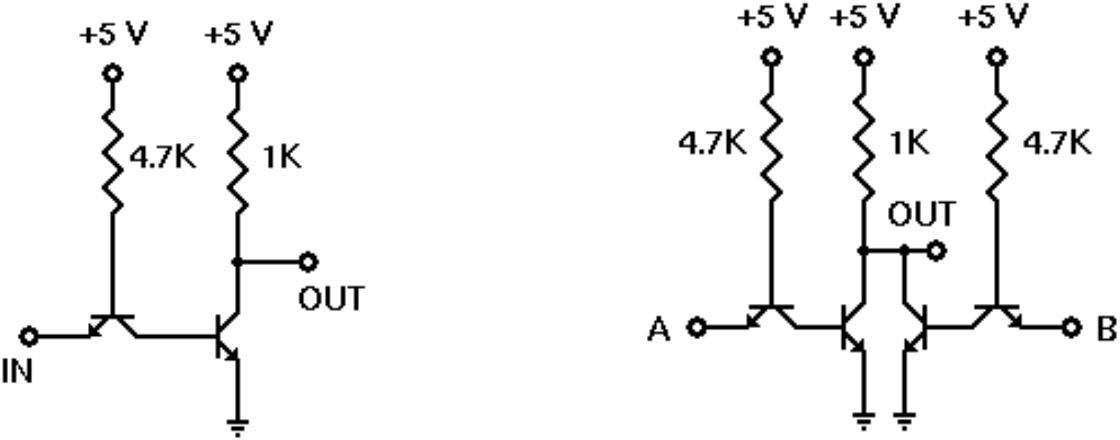
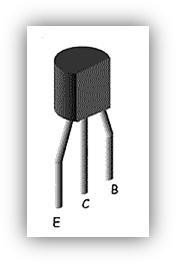


Fig 9: TTL Inverter Fig 10: 2-input TTL NOR gate

**BJT pin configuration:**



**Pre-Lab Homework:**

Explain how n-p-n BJT transistors work?

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

# Apparatus:

|  |  |  |
| --- | --- | --- |
| 1. | 2N4124 NPN silicon transistor (or equivalent). | |
| 2. | Resistors | 15KΩ, 1KΩ, 4.7 KΩ |

1. Connecting wires.
2. Trainer Board

# Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within VDD) to turn on the transistors and/or chip, otherwise it may get damaged.

# Experimental Procedure:

1. Set up the circuit for RTL inverter as shown in Fig.7.
2. For each input combination, find the output and place them in a Truth Table. The Truth Table should have two sets of outputs- one ideal and one experimental.
3. Repeat steps 1 and 2 for each circuit set-up from Fig.8 to Fig. 10.

# Results and Discussion:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

# Report:

1. For, each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?

Answer:

**RTL Inverter:** This is an [inverter](http://en.wikipedia.org/wiki/Inverter_%28logic_gate%29) implemented using [resistor-transistor logic](http://en.wikipedia.org/wiki/Resistor-transistor_logic), the earliest form of logic implemented with transistors. When the input is high, the output is low, and vice versa.

When the input is high (3.6 V), a current flows from the base to the emitter. The transistor wants the collector-emitter current to be 100 times the base current, but it can't, because the collector is connected to the same voltage through a larger resistor. So, the transistor is in saturation mode; it gets the collector voltage down to the saturation voltage of 9.7 mV.

When the input is low (at ground), no current flows through the base, so the transistor is off, and the collector stays at 3.6 V.

**4-input RTL Inverter:** With all four logic inputs set to logic 0, all four transistors are turned off. The resulting output is therefore a logic 1. With all other input combinations, at least one input is a logic 1, and the corresponding transistor is therefore turned on. This pulls the output voltage down to a logic 0.

Having more transistors turned on makes no difference; the output cannot be pulled down any harder or any further. It remains at logic 0.

This gate is therefore verified to perform a logical NOR function upon its input signals.

When you have completed this experiment, leave your experimental circuit in place for the next experiment. You will be extending it without making any changes to the present circuit.

**TTL Inverter:**

We should have found that this circuit performed a logic inversion, or NOT function. With a logic 0 input, it produced a logic 1 output. With a logic 1 input, it produced a logic 0 output. Thus, this circuit is indeed an inverter, as expected. When We have completed this experiment, make sure power to your experimental circuit is turned off.

**2-input TTL NOR gate**:

With this circuit, we found that one of the outputs indicated that the gate would output a logic 1 only when both inputs were at logic 0. The moment either input became a logic 1, the output dropped to logic 0. This is the correct behavior for a NOR gate, so this circuit does indeed perform the function it was intended to perform. When we have completed this experiment, make sure power to experimental circuit is turned off. Remove all experimental components from your breadboard socket and put them aside for use in other experiments.

1. Design RTL 4-input OR gates.

RTL 4-input OR gate:

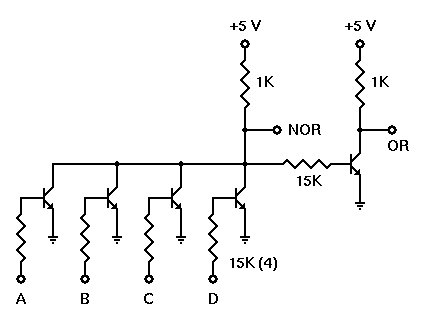


Figure 11: RTL 4-input OR gate

One of the output produced exactly the same output pattern as it did in the previous experiment: logic 1 when all switches were set to logic 0, and logic 0 all the rest of the time. Thus, the addition of the inverter circuit did not affect the output state of the NOR gate.

Another output showed the opposite state from one of the output at all times, indicating that this is indeed an inverter circuit, just like the inverter you built and tested in your first RTL experiment. Thus, another output showed a logic 0 when all switches were at logic 0, and a logic 1 for all other switch combinations. This is correct OR gate behavior, showing that this circuit operates correctly for all possible input states.

This concludes our experiments with RTL gates. Make sure you have power turned off, and then remove all of the experimental components from your breadboard socket.

1. Design 2-input TTL NAND and NOR gates.

2-input TTL NAND:

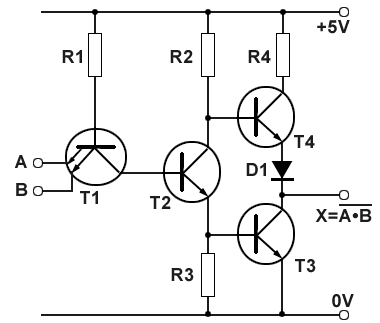


Figure 12: 2-input TTL NAND gate

2-input TTL NOR gates:

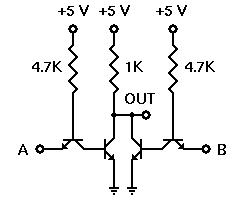


Figure 13: 2-input TTL NOR gate

# Reference(s):

# Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.

# Boylestad, Robert L. *Electronic devices and circuit theory*. Pearson Education India, 2009.

# Simulation Results:

# Simulation for the mentioned circuit are given below:

# Diode Logic OR gate:

# Circuit Diagram:

# 

# Figure 14: Diode Logic OR gate

# Simulated Results:

# 

# Diode Logic AND gate:

# Circuit Diagram:

# 

# Figure 15: Diode Logic AND gate

# Simulated Results:

# 

# 2 input Diode Logic AND-OR gate:

# Circuit Diagram:

# 

# Figure 16: Two input Diode Logic AND-OR gate

# Simulated Results:

# 